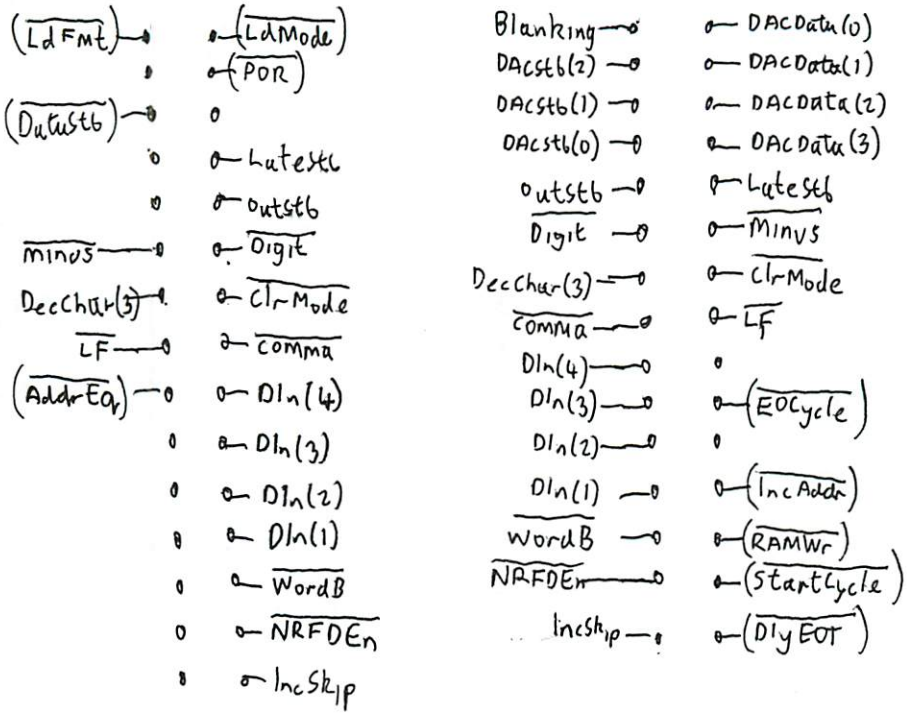
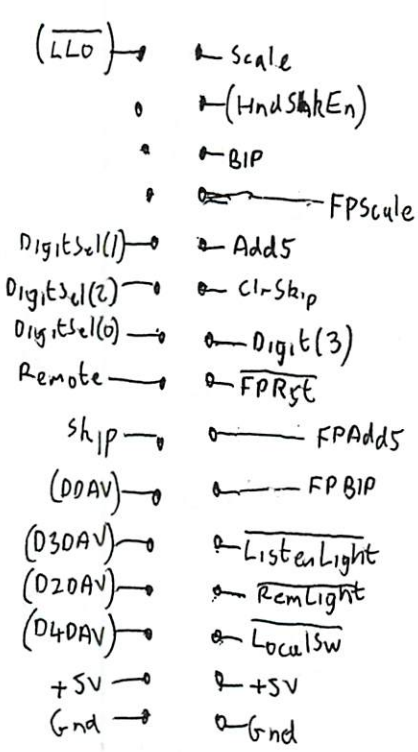
HP59303

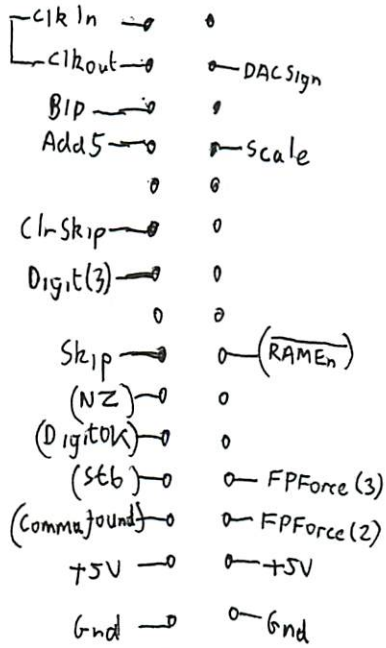
Rear

LHS



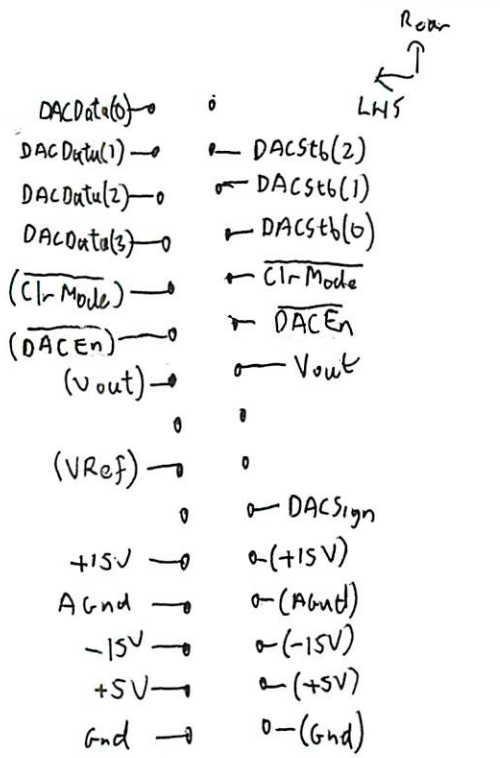


MPIB PCB

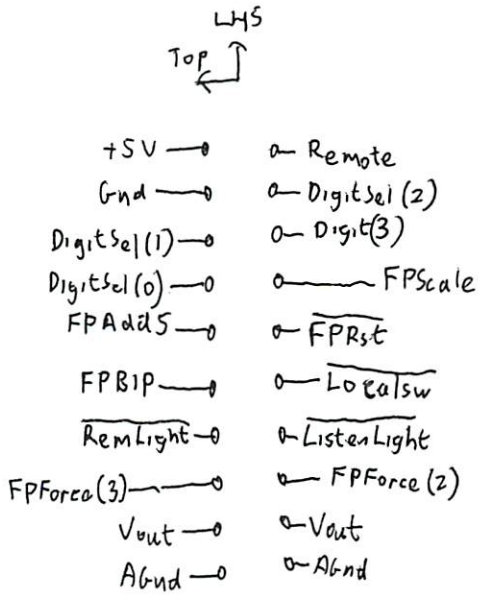


Data PCB

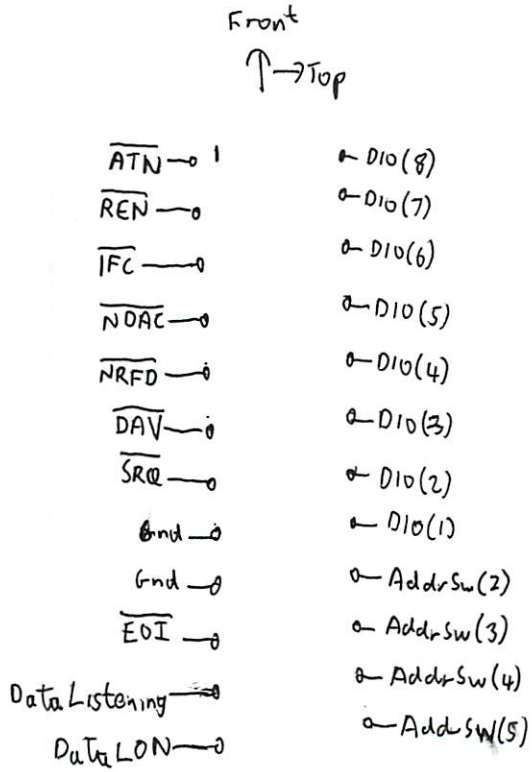
HP59303



DAC PCB

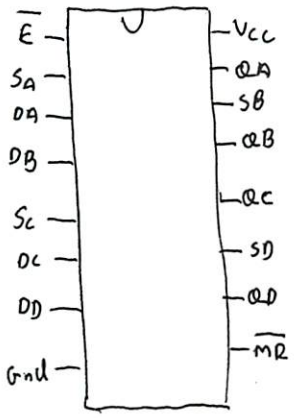


Front panel PCB



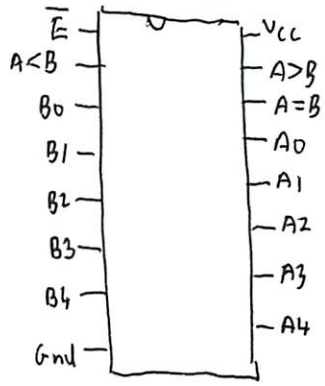
HPIB Connector PCB

→ HPIB PCB



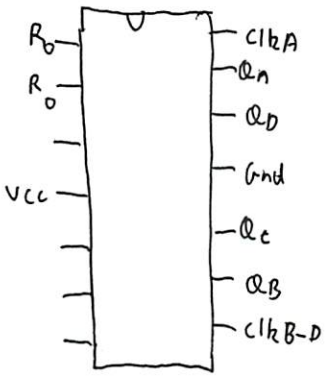
93L14

4-bit Latch



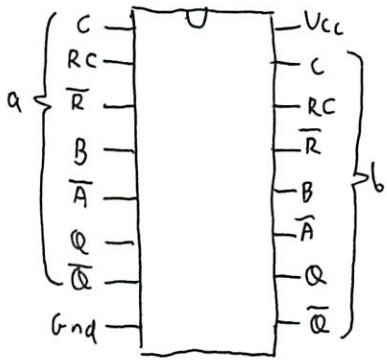
9324

5-bit Comparator



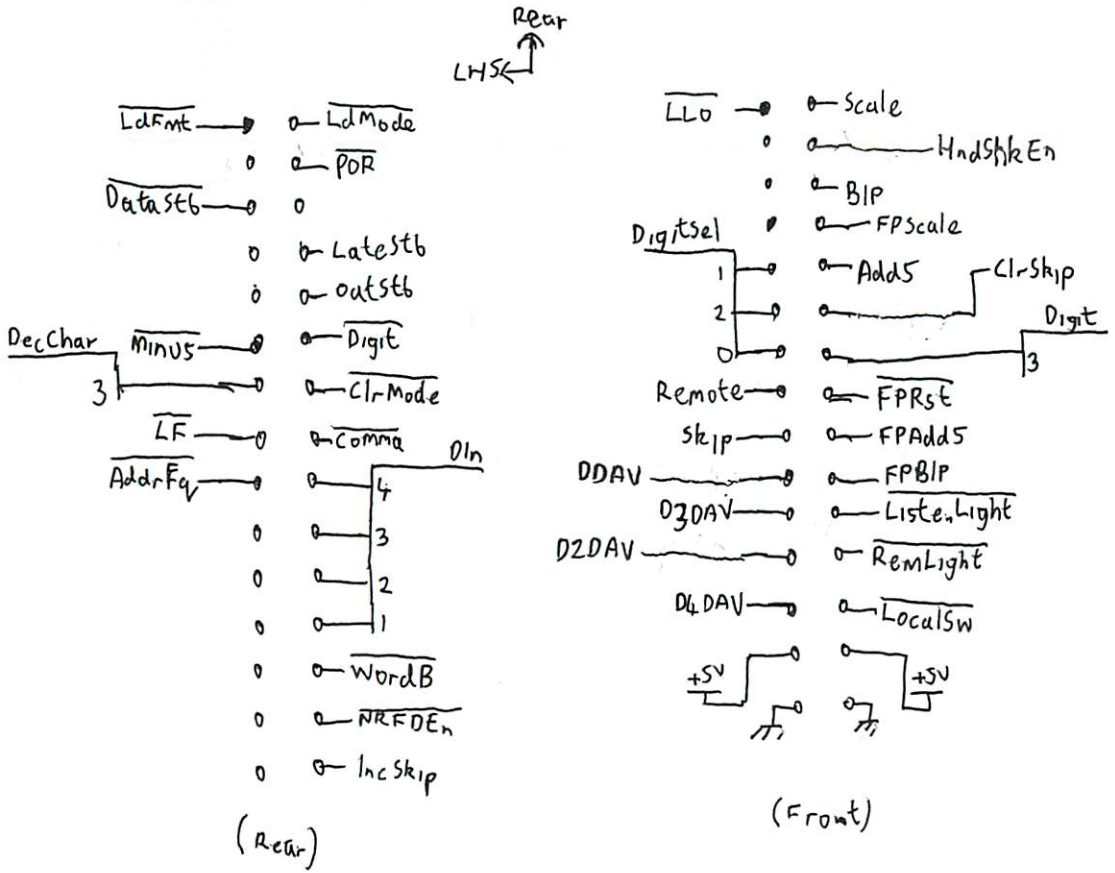
74L93

Not as '93

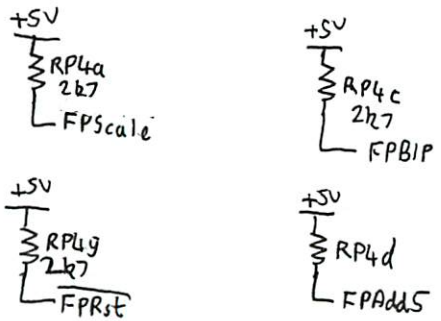


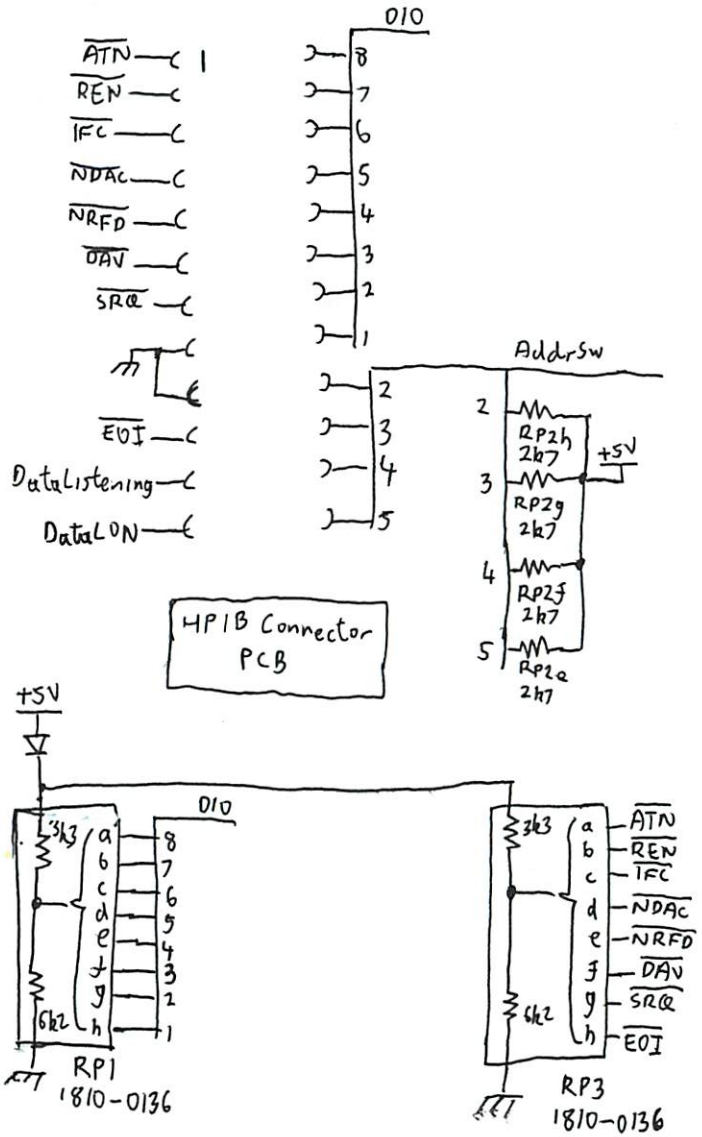
96L02

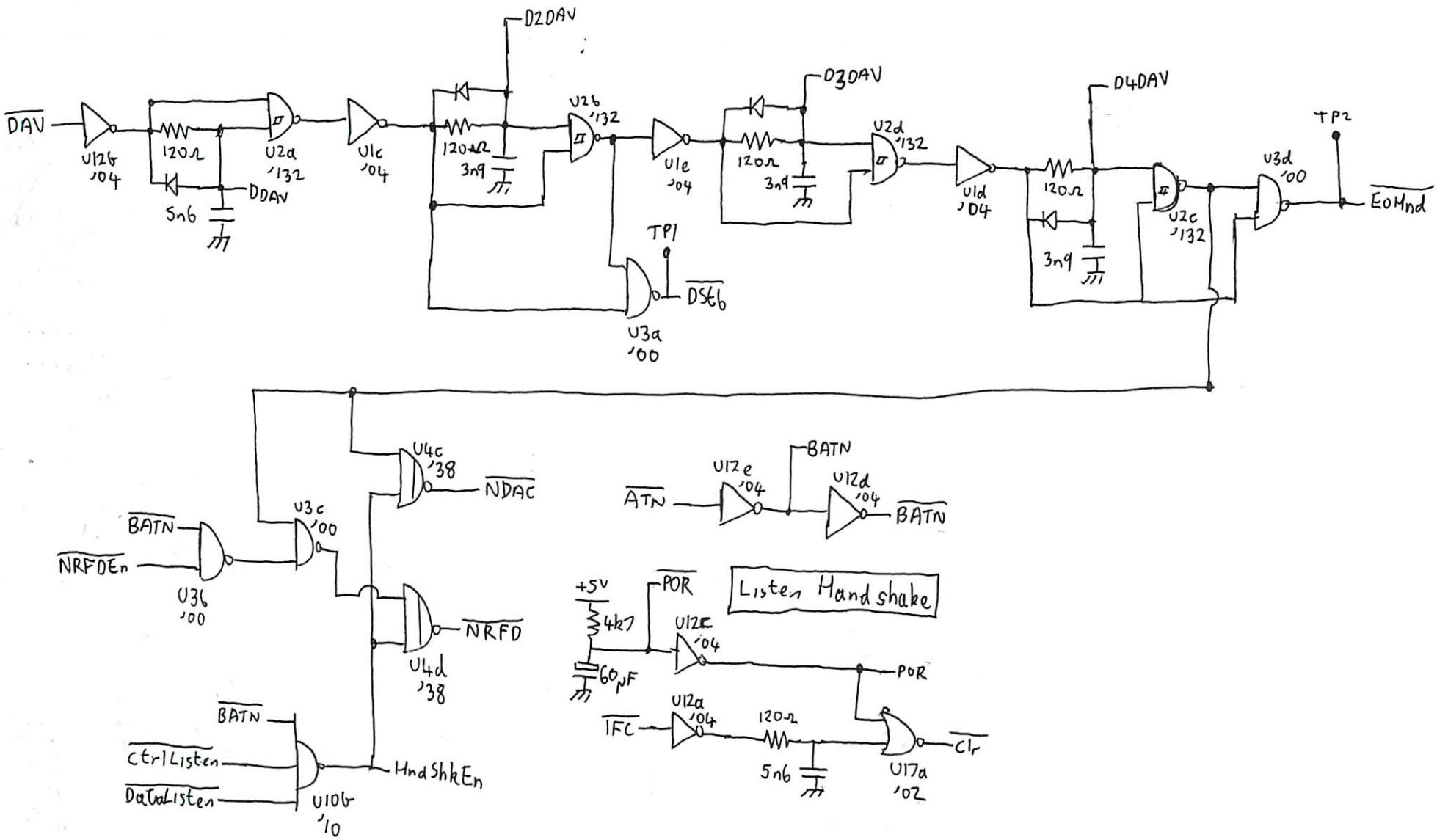
Dual Monostable

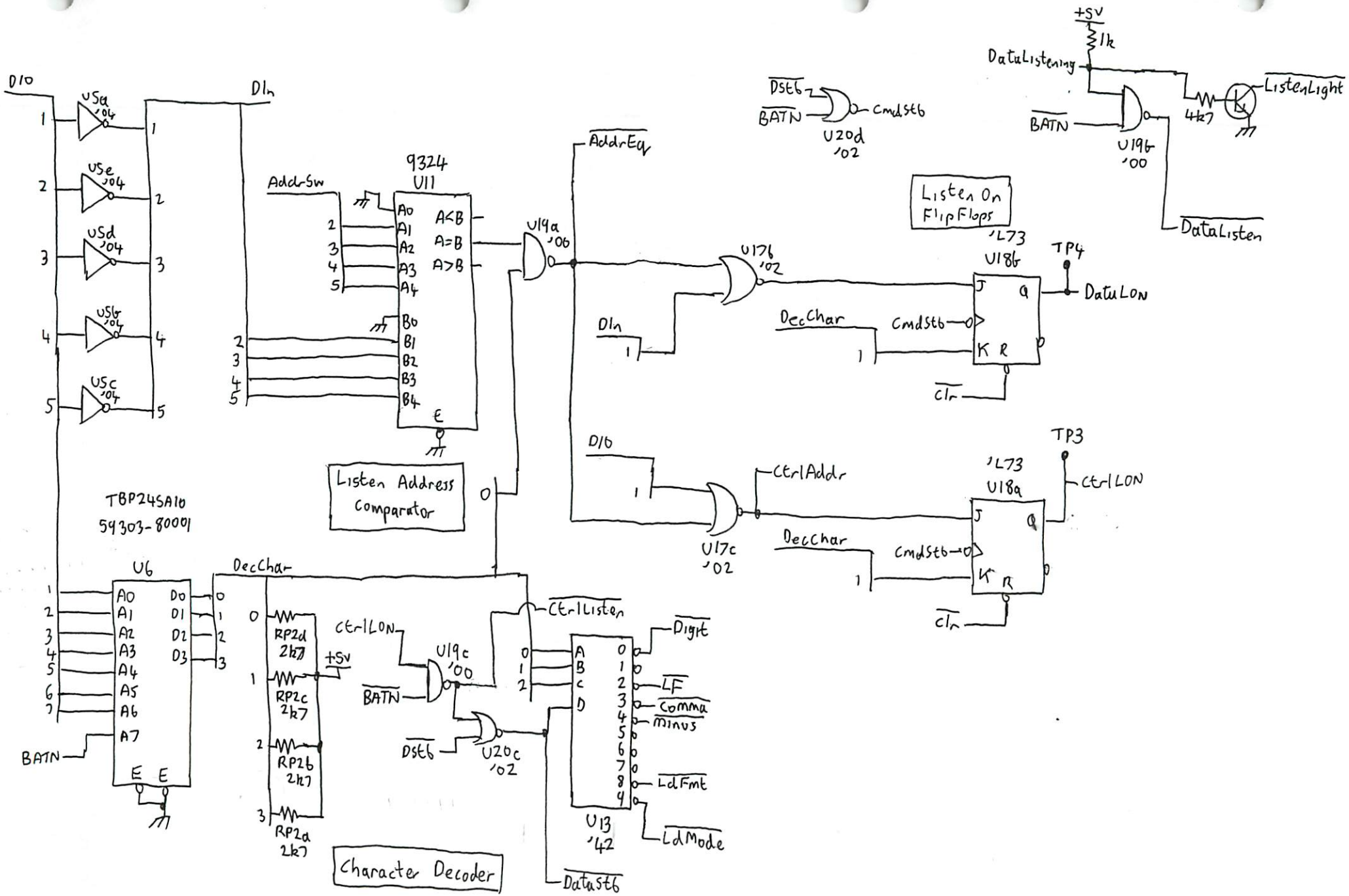


Backplane connectors



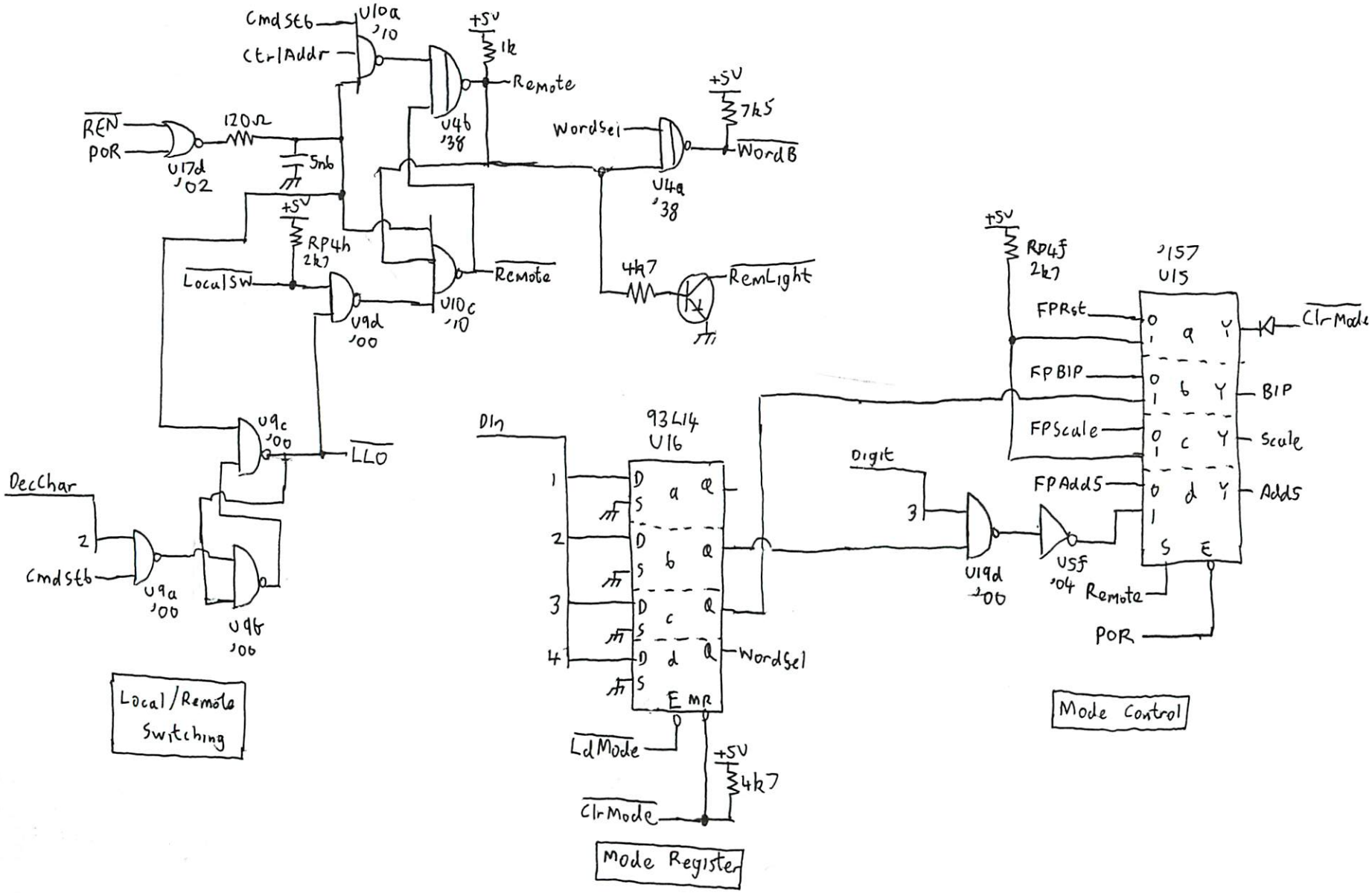



DAV
U12b '04
120Ω
5n6
DDAV
U2a '132
U1c '04
D2DAV
120Ω
3n9
U2b '132
U1e '04
TP1
DStb
U3a '00
D3DAV
120Ω
3n9
U2d '132
U1d '04
D4DAV
120Ω
3n9
U2c '132
U3d '00
TP2
EoHnd
U4c '38
NDAC
U3c '00
BATN
NRFDEn
U3b '00
U4d '38
NRFD
BATN
CtrlListen
DataListen
U10b '10
HndShkEn
ATN
U12e '04
BATN
U12d '04
BATN
Listen Handshake
+5V
4k7
60pF
POR
U12f '04
POR
IFC
U12a '04
120Ω
5n6
U17a '02
Clr

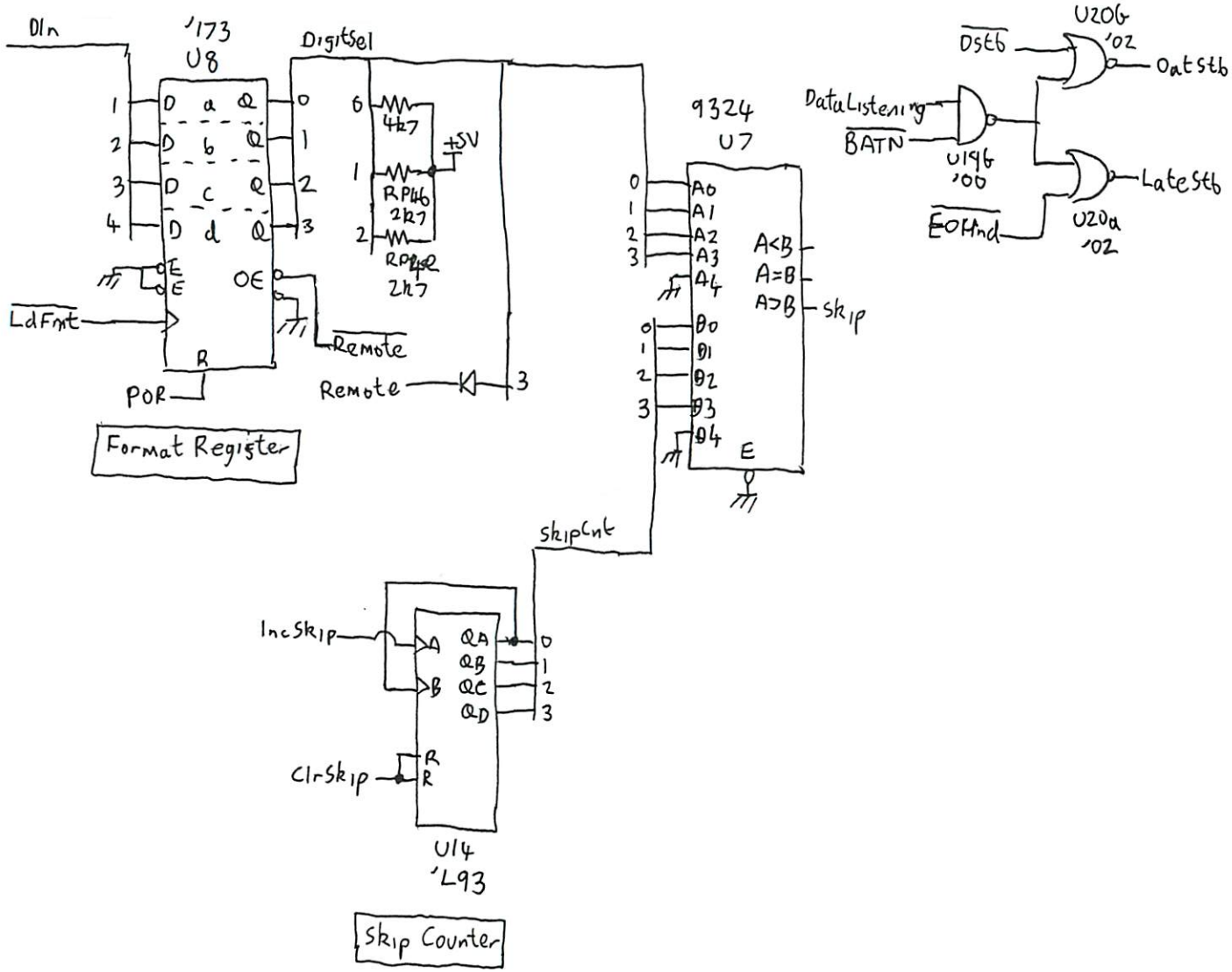


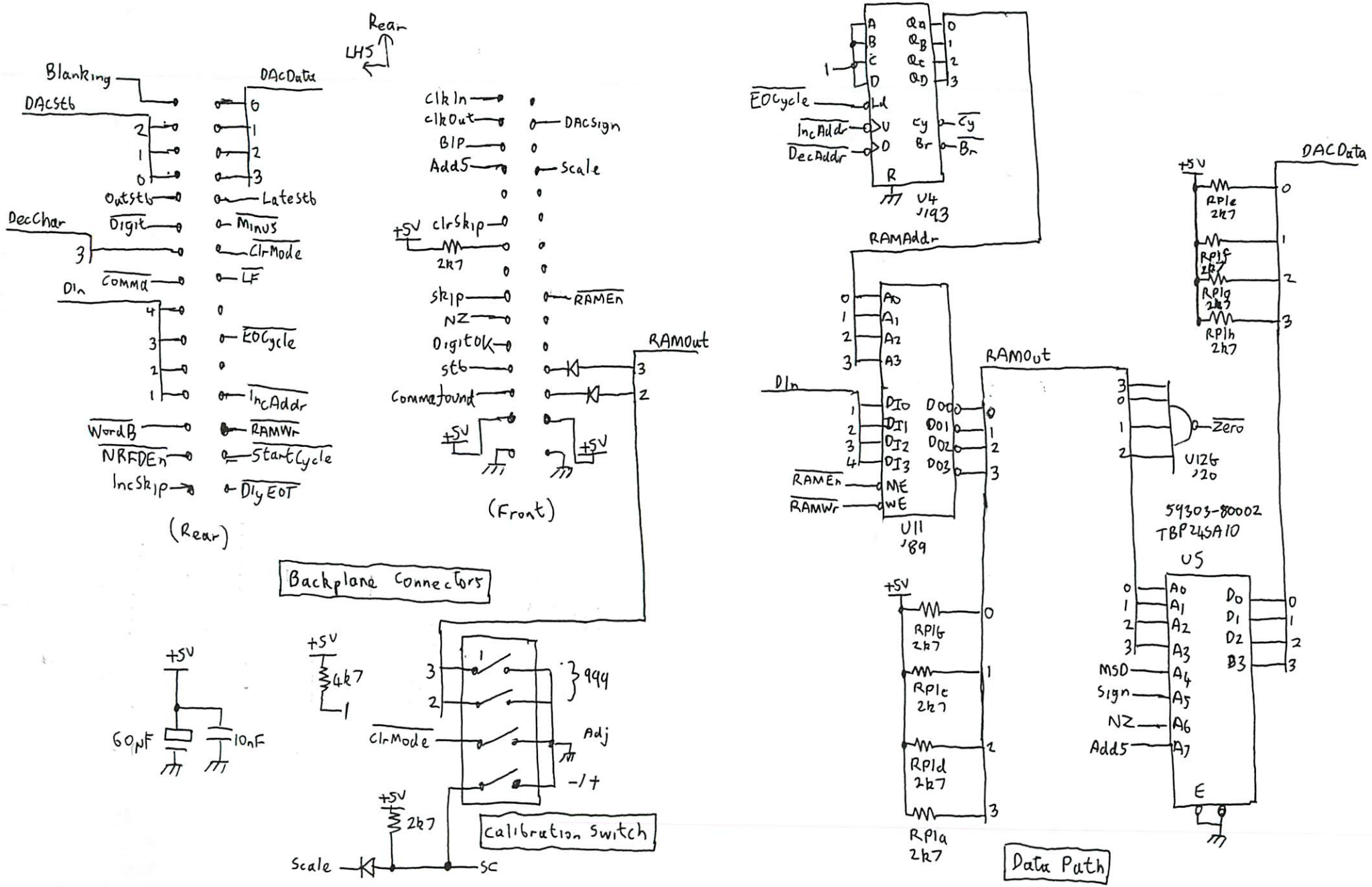
HP59303 HPIB PCB Sheet (3)

59303-60001



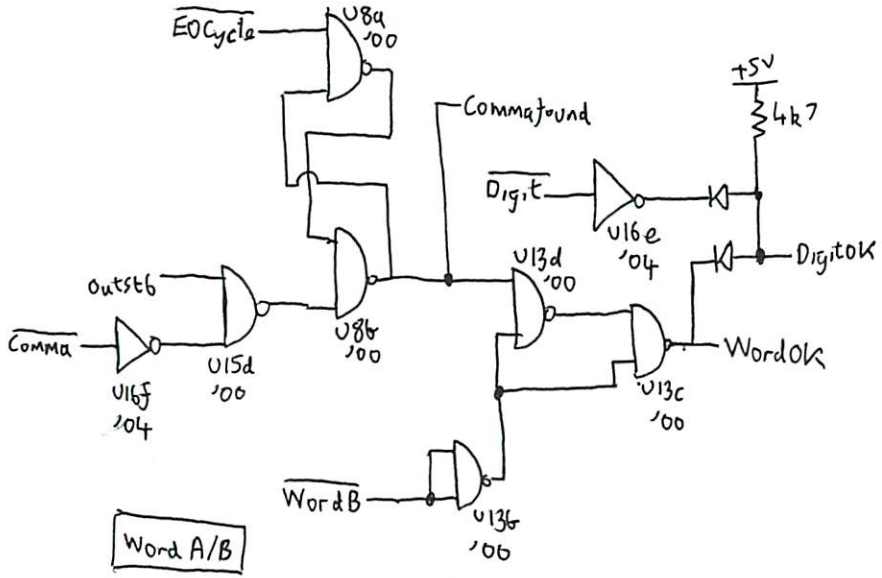
HP 59303 HPIB PCB Sheet (4) 59303-60001

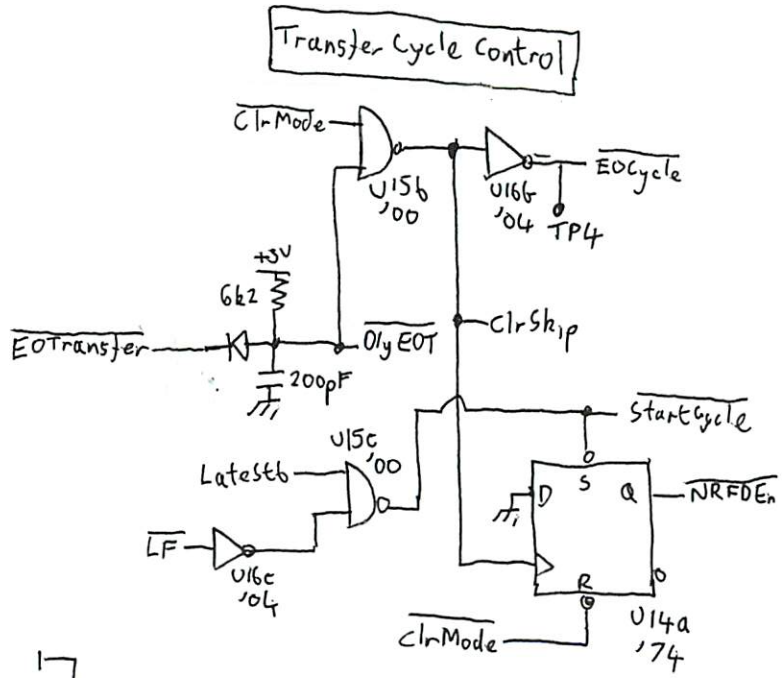

DIn
'173
U8
DigitSel
9324
U7
U206
'02
DStb
OatStb
DataListening
BATN
U196
'00
LateStb
EOIAnd
U20a
'02
LdFmt
POR
Remote
Remote
4k7
+5V
RP46
2k7
RP45
2k7
A<B
A=B
A>B
Skip
SkipCnt
IncSkip
ClrSkip
U14
'L93
Format Register
Skip Counter

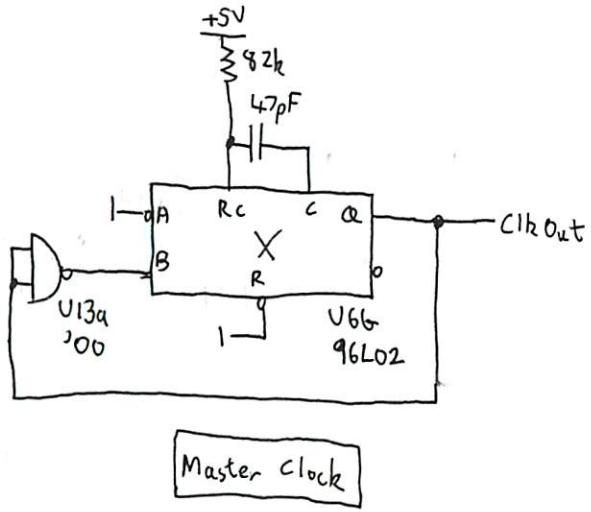


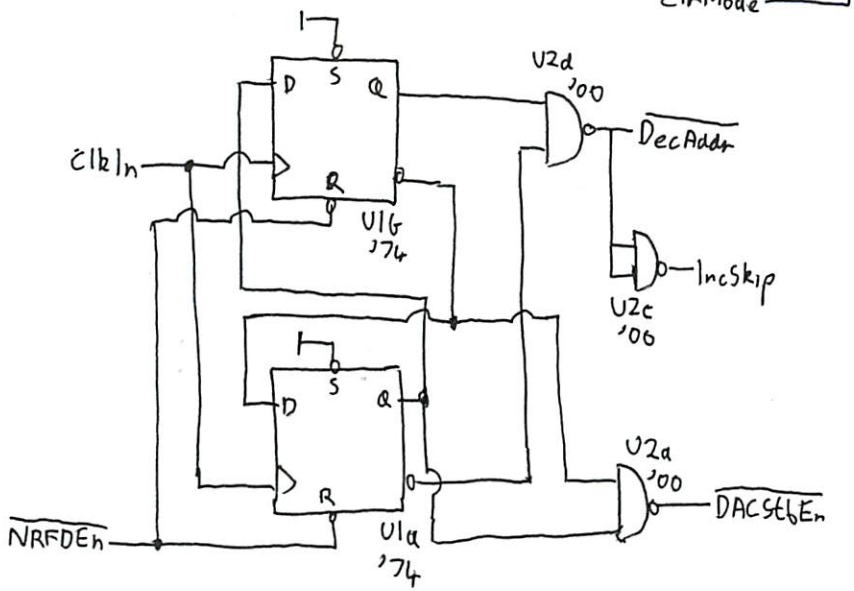
HP 59303 Data PCB Sheet (1)

59303-60002

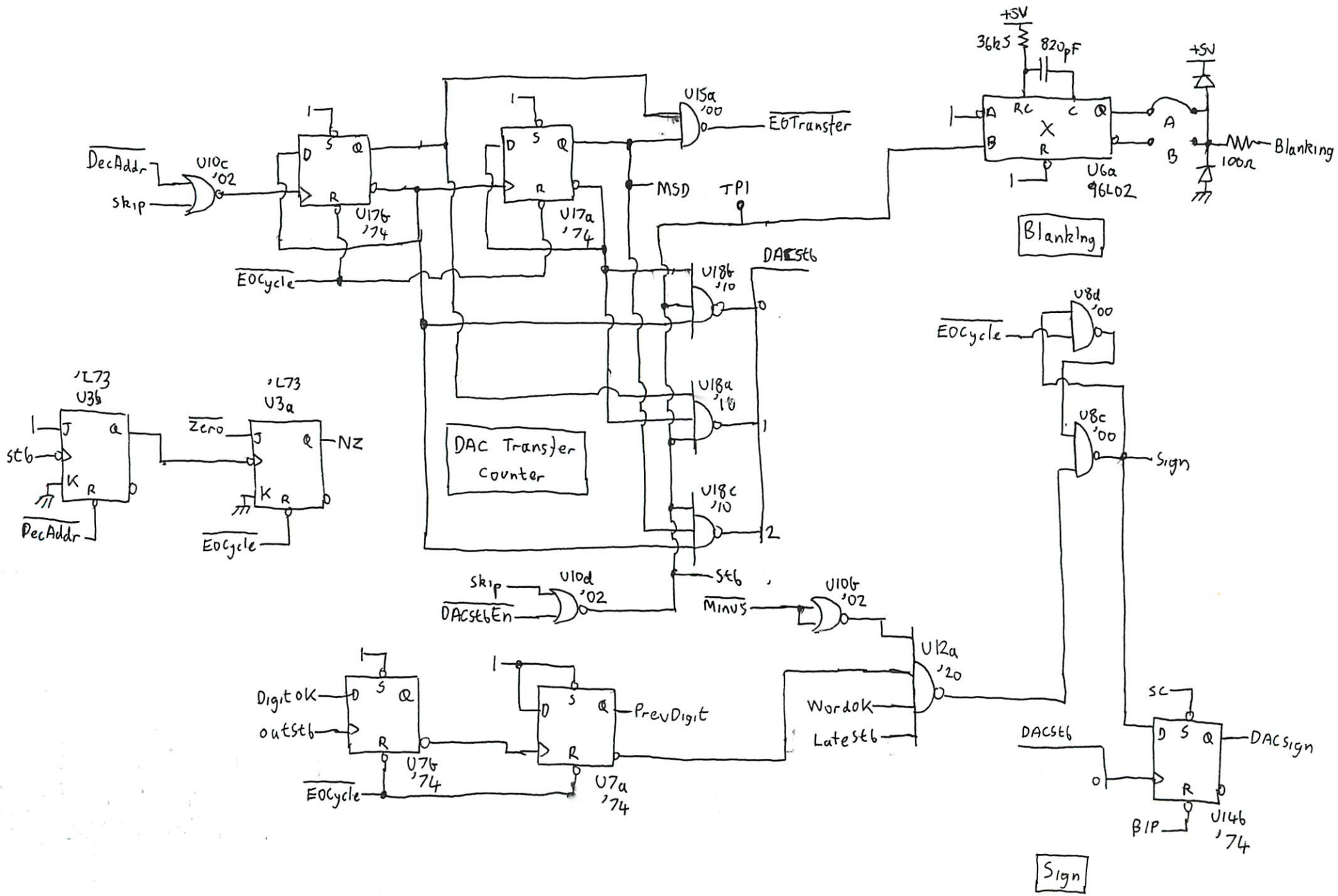




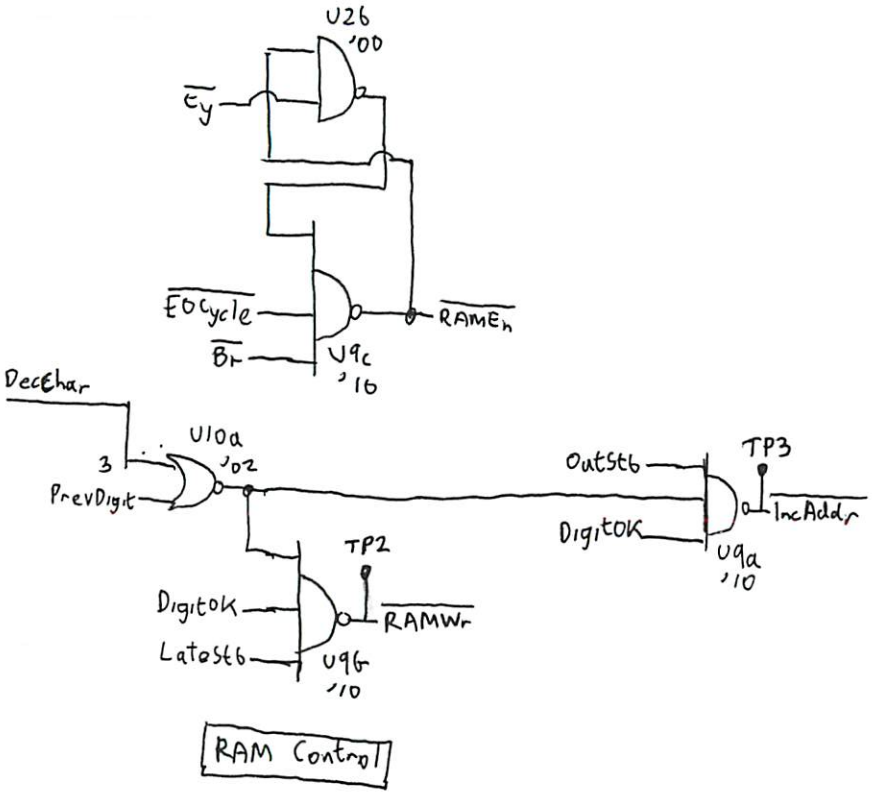


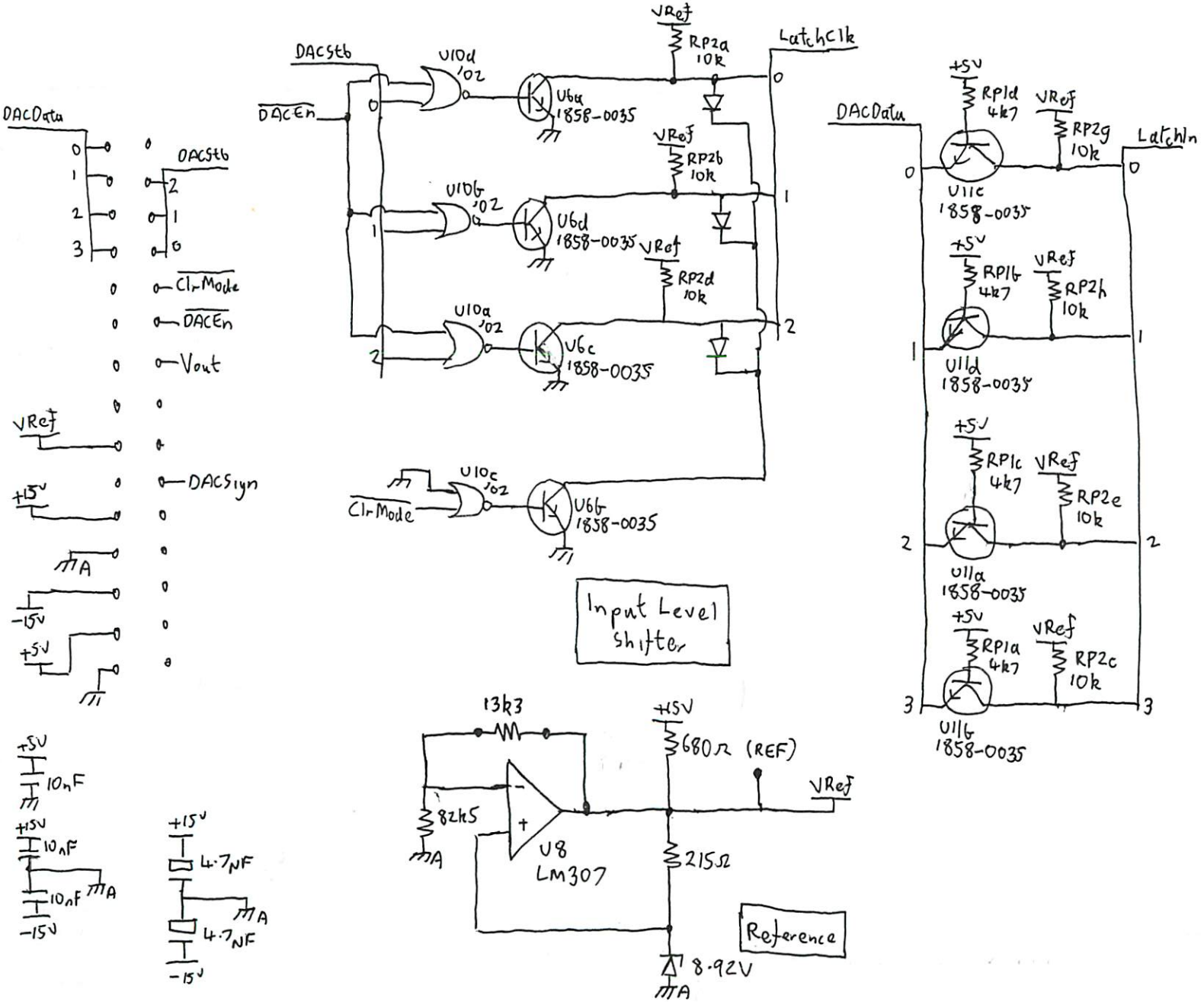


HP 59303 Data PCB Sheet (2) 59303 - 60002

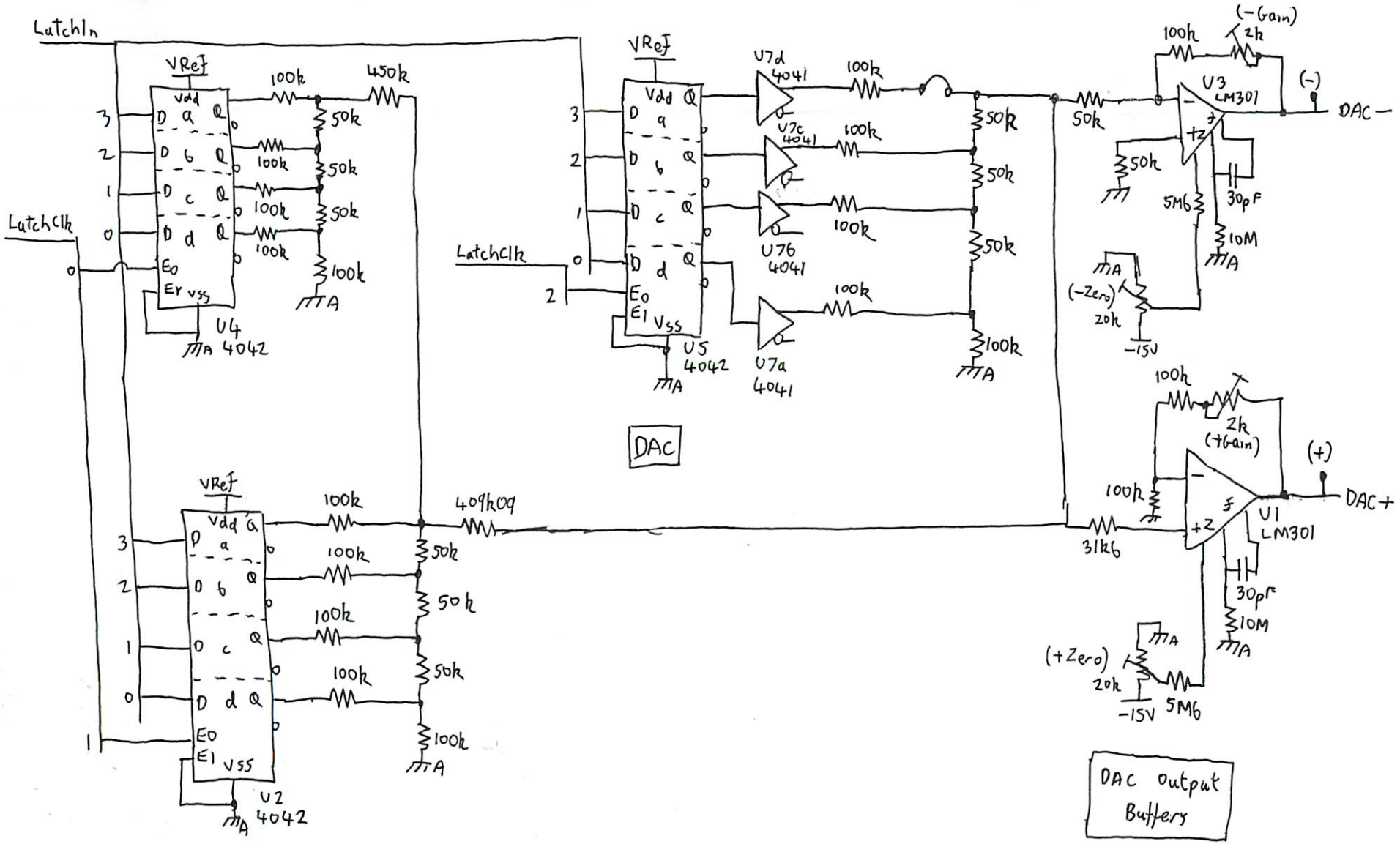


HP59303 Data PCB Sheet (3) 59303-60002

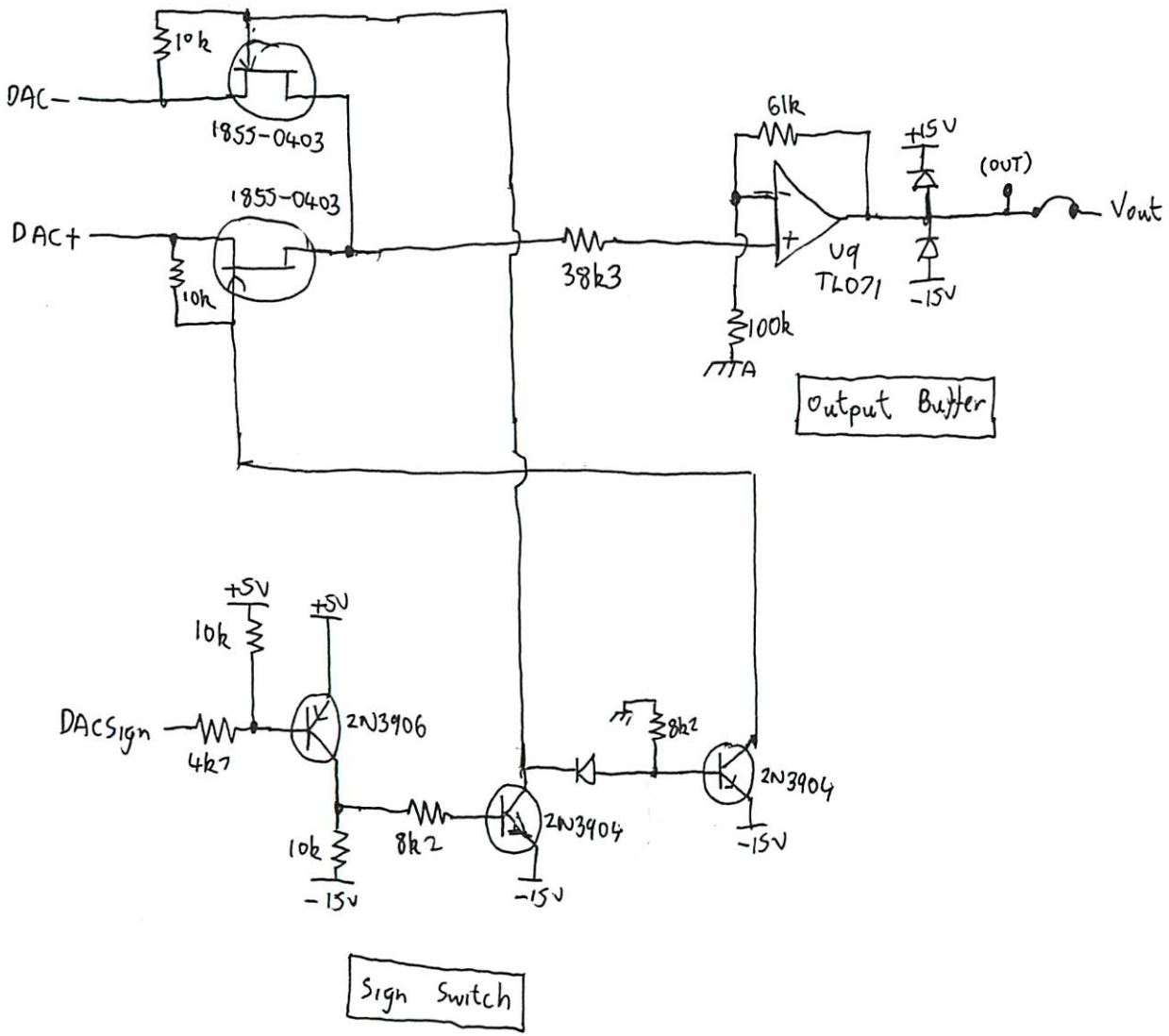

U26
'00
$\overline{Ey}$
$\overline{EOcycle}$
$\overline{Br}$
U9c
'16
$\overline{RAMEn}$
DecEhar
3
PrevDigit
U10a
'02
TP2
DigitOK
LatoSt6
U9b
'10
$\overline{RAMWr}$
OutSt6
DigitOK
U9a
'10
TP3
$\overline{IncAddr}$
RAM Control



HP 59303 DAC PCB Sheet (1) 59303-60003



HP 59303 DAC PCB Sheet (2) 59303-60003

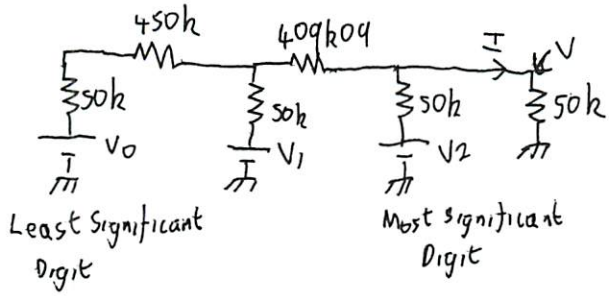

10k
DAC−
1855-0403
1855-0403
DAC+
10k
38k3
61k
+15V
(OUT)
Vout
U9
TL071
-15V
100k
A
Output Buffer
+5V
+5V
10k
DACSign
4k7
2N3906
10k
8k2
-15V
2N3904
8k2
2N3904
-15V
Sign Switch

Theory of DAC combination

HP59303

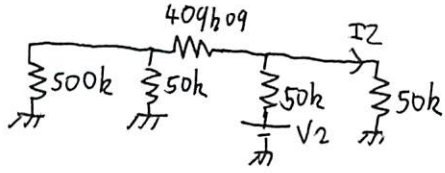
DAC consists of 3 R-2R ladders, 1 for each decade.

Output impedance of each DAC = 50kΩ. They are combined as shown on DAC PCB diagram sheet (2). So, representing each DAC as a voltage source in series with 50kΩ, the combination is equivalent to:



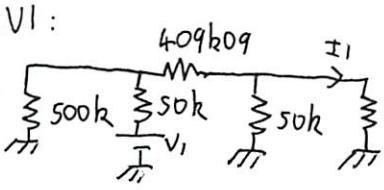
Using the superposition principle:

for V_2 :



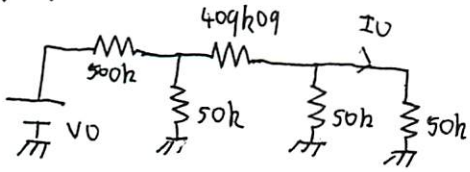
$\rightarrow I2 = (V2, 0.00947)\,mA$

for V1 :



$\rightarrow I1 = (V_1 . 0.000947)\,mA$

for V0 :



$\rightarrow I0 = (V_0 . 0.0000947)\,mA$

So $I = I_0 + I_1 + I_2 = 0.000947\,(V_0 + 10V_1 + 100V_2)\,mA$

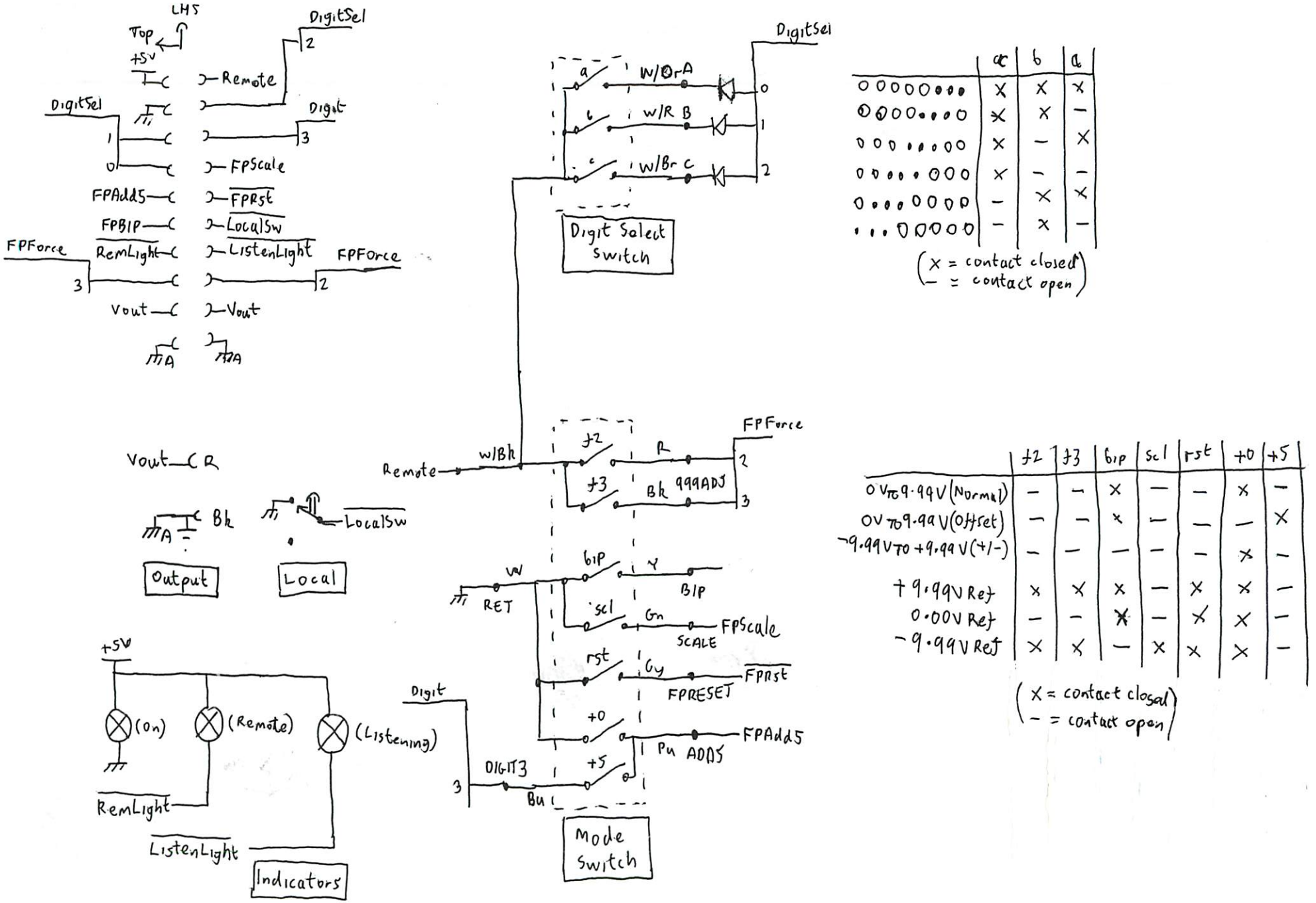
$V = 50.I = 0.00474\,(V0 + 10V_1 + 100V_2)$.

$V_{Ref} = 10.36V$

DAC Set to 999 $\rightarrow$ DAC output (at pin 3 of U1, say) $= \frac{V_{Ref} \cdot 999 \cdot 0.00474}{16} = 3.07\,V$

At TP(+) $\rightarrow \approx 2 \times$ DAC output $= 6.14V$.

At output $\rightarrow \approx 6.14 \times \frac{161}{100} \approx 9.9V$



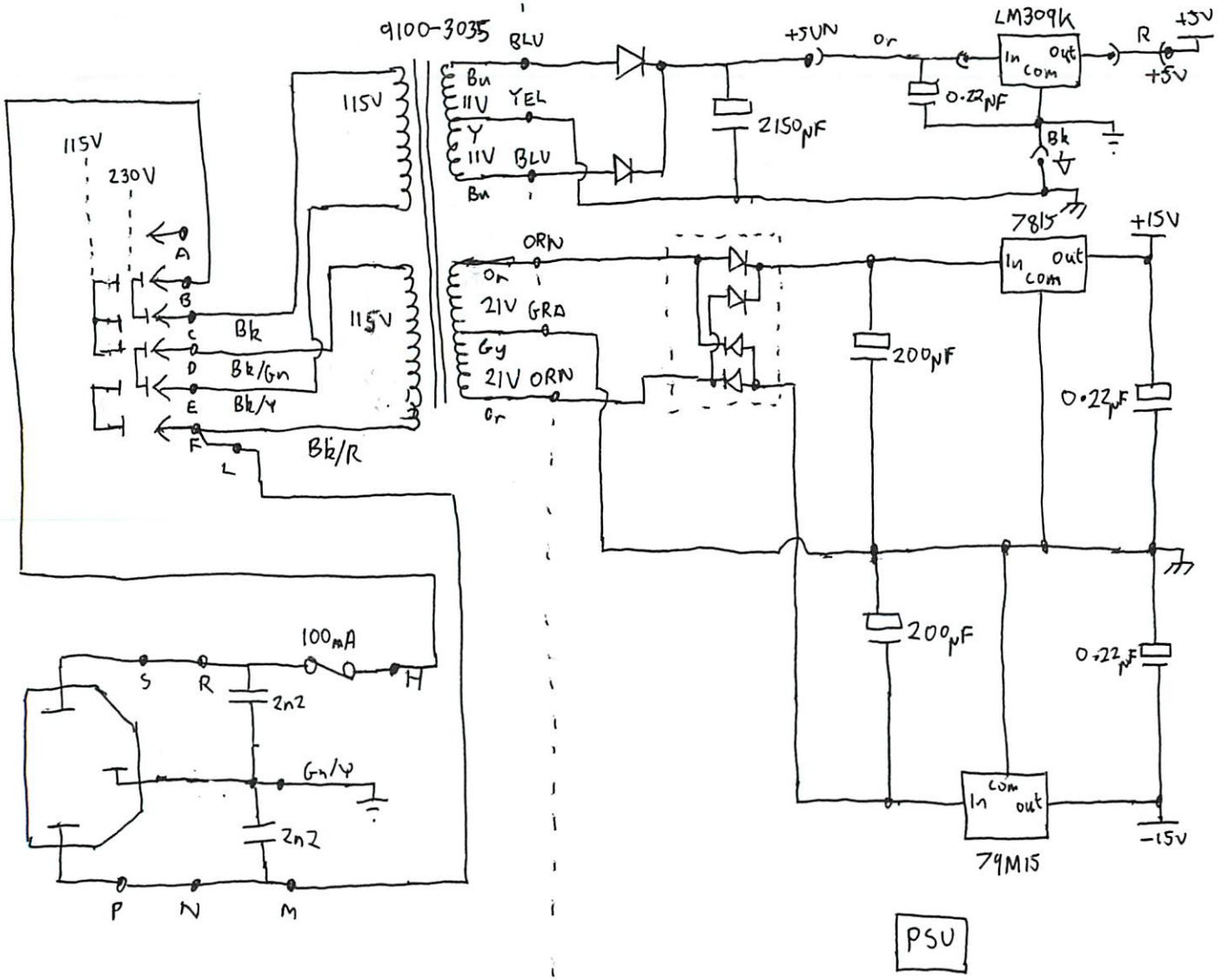
	a	b	c
0	X	X	X
1	X	X	–
2	X	–	X
3	X	–	–
4	–	X	X
5	–	X	–

(X = contact closed
– = contact open)

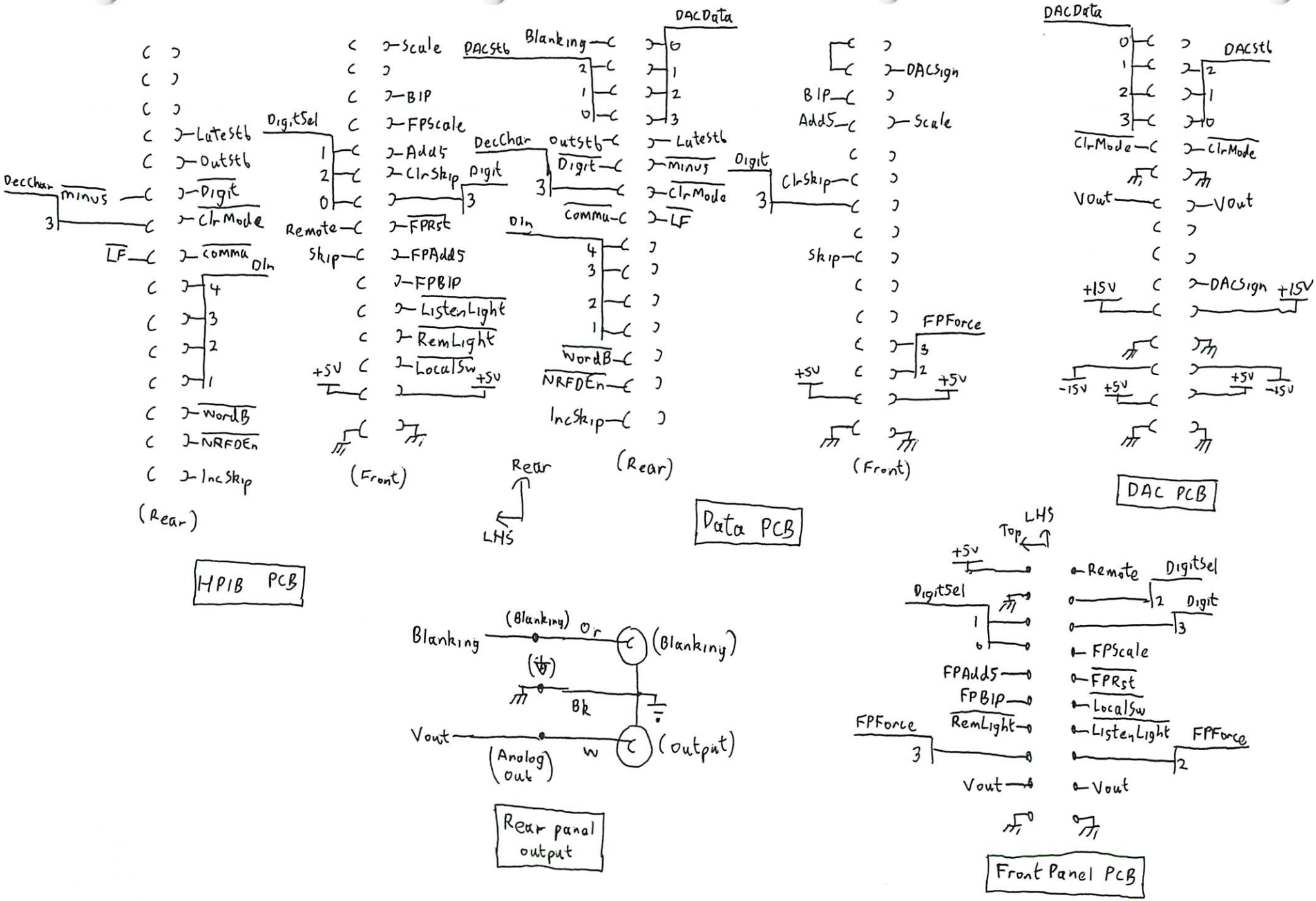
	+2	+3	BIP	scl	rst	+0	+5
0V to 9.99V (Normal)	–	–	X	–	–	X	–
0V to 9.99V (Offset)	–	–	X	–	–	–	X
−9.99V to +9.99V (+/−)	–	–	–	–	–	X	–
+9.99V Ref	X	X	X	–	X	X	–
0.00V Ref	–	–	X	–	X	X	–
−9.99V Ref	X	X	–	X	X	X	–

(X = contact closed
– = contact open)

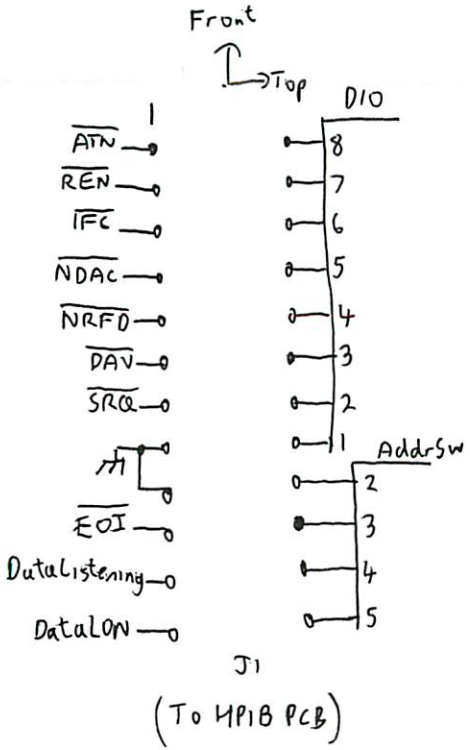
HP59303 Front Panel PCB 59303-60004

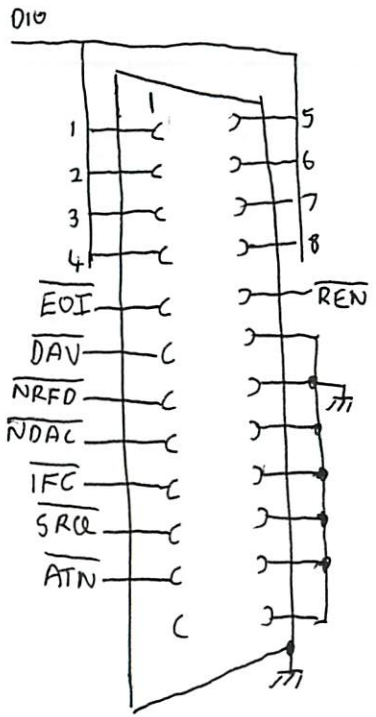


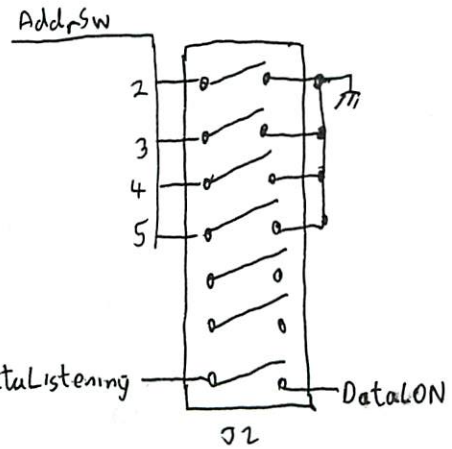
HP 59303 Backplane Sheet (1) 59303 - 60005



HP59303 Backplane Sheet (2) 59303-60005







HP59303 HPIB Connector PCB 59303-60006